

DERWENT-ACC-NO: 1993-206853

DERWENT-WEEK: 199611

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TITLE: Flip=chip bonded defective resin encapsulated semiconductor die replacement method for direct chip attachment package- leaving part of the encapsulation resin and part of solder bump electrodes, enclosed in resin, on substrate by milling planarisation after mechanical die removal to form mesa base on substrate

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PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAINIPC |
|----------------------|--------------------|----------|-------|-------------|
| EP 548603 A1 | June 30, 1993 | E | 008 | H01L 021/60 |
| US 5488200 A | January 30, 1996 | N/A | 008 | H05K 001/18 |
| <u>JP 05251516 A</u> | September 28, 1993 | N/A | 000 | H01L 021/60 |
| US 5355580 A | October 18, 1994 | N/A | 007 | H05K 003/39 |
| EP 548603 B1 | September 27, 1995 | E | 009 | H01L 021/60 |
| DE 69205134 E | November 2, 1995 | N/A | 000 | H01L 021/60 |

DESIGNATED-STATES: DE FR GB DE FR GB

CITED-DOCUMENTS: 05Jnl.Ref; 5.Jnl.Ref

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO | APPL-DATE |
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| EP 548603A1 | N/A | 1992EP0120518 | December 2, 1992 |
| US 5488200A | Div ex | 1992US0976619 | November 16, 1992 |
| US 5488200A | N/A | 1994US0255596 | June 8, 1994 |
| US 5488200A | Div ex | US 5355580 | N/A |
| JP 05251516A | N/A | 1991JP0344822 | December 26, 1991 |
| US 5355580A | N/A | 1992US0976619 | November 16, 1992 |
| EP 548603B1 | N/A | 1992EP-0120518 | December 2, 1992 |
| DE 69205134E | N/A | 1992DE0605134 | December 2, 1992 |
| DE 69205134E | N/A | 1992EP0120518 | December 2, 1992 |
| DE 69205134E | Based on | EP 548603 | N/A |

INT-CL (IPC): H01L021/60, H05K001/18 , H05K003/39

ABSTRACTED-PUB-NO: EP 548603A

BASIC-ABSTRACT:

The method involves replacing a semiconductor chip (4) bonded facedown to a substrate (2) by bump electrodes (6) with the space between chip bottom and substrate filled with encapsulation resin (14). The chip is mechanically removed from the substrate with a cutting end mill (26).

The surface of the resin and the bump electrodes remaining on the substrate are planarised pref. with a finishing end mill to a height about half the original bump electrode height. Another chip is aligned and bonded to the bump electrodes on the substrate, using other bump electrode attached to the replacement die. The space between the bottom surface of the replacement chip and the substrate is filled with encapsulation resin.

ADVANTAGE - Simple chip replacement with minimal chemical or mechanical damage to substrate or circuits and components; maintains reliable connection after replacement, with improved thermal stress resistance.

ABSTRACTED-PUB-NO: EP 548603B

EQUIVALENT-ABSTRACTS:

A method for replacing a semiconductor chip (4,4A) bonded face down to a substrate (2) by bump electrodes (6,6A) with the space between the bottom surface of said semiconductor chip and said substrate being filled with an encapsulation resin (10), comprising the steps of; mechanically removing said chip from said substrate, planarising the surface of said resin and said bump electrodes remaining on said substrate, bonding another chip to the bump electrodes on said substrate through the use of other bump electrodes, and filling the space between the bottom surface of said another chip and said substrate with an encapsulation resin.

US 5355580A

The space between the bottom surface of a semiconductor chip and a substrate is filled with an encapsulation resin. The chip is mechanically removed from the substrate. The surface of the resin is planarised, the bump electrodes remaining on the substrate.

Another chip is bonded to the bump electrodes on the substrate through the use of other bump electrodes. The space between the bottom surface of the other chip and substrate is filled with an encapsulation region. The removal of the chip is accomplished by milling.

USE - For replacing a semiconductor chip bonded face down to a substrate by bump electrodes, esp. in a direct chip attachment (DCA) packaging system.

US 5488200A

An interconnect structure, comprising:

a first substrate with a surface;

a pattern of multiple conductive pads defining an area on the surface of the first substrate;

conductive bumps with first ends positioned on the conductive pads, and second ends of the bumps defined by a second surface approximately parallel to and above the surface of the first substrate and which defines the flat, distal ends of the bumps wherein the second surface is mountable to an electronic device having additional conductive bumps; and a first layer of an encapsulant filling around the bumps in the volume defined by the area of the pattern of conductive pads and between the first substrate surface and the defining second surface.

CHOSEN-DRAWING: Dwg.2/6 Dwg.6/6 Dwg.4/6 Dwg.4/6

TITLE-TERMS: BOND DEFECT RESIN ENCAPSULATE SEMICONDUCTOR DIE REPLACE METHOD
DIRECT CHIP ATTACH PACKAGE LEAVE PART ENCAPSULATE RESIN PART SOLDER
BUMP ELECTRODE ENCLOSURE RESIN SUBSTRATE MILL PLANE AFTERMECHANICAL
DIE REMOVE FORM MESA BASE SUBSTRATE

DERWENT-CLASS: U11 U14

EPI-CODES: U11-E01C; U11-E02B; U14-H03A1; U14-H03A2; U14-H04B9;

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